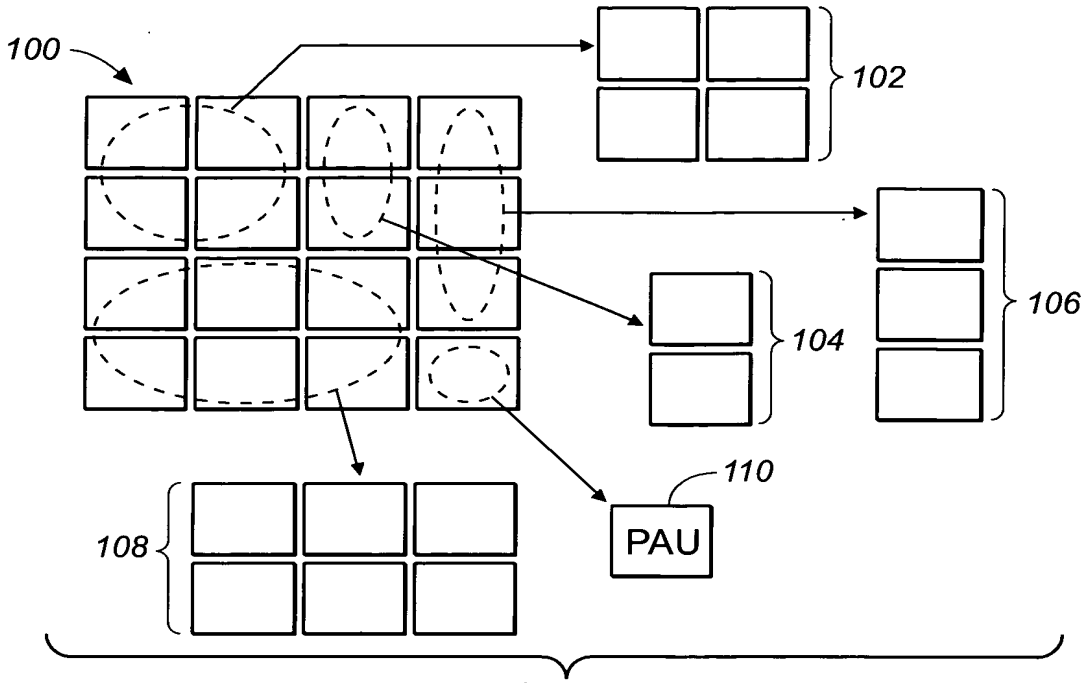

FIG._1

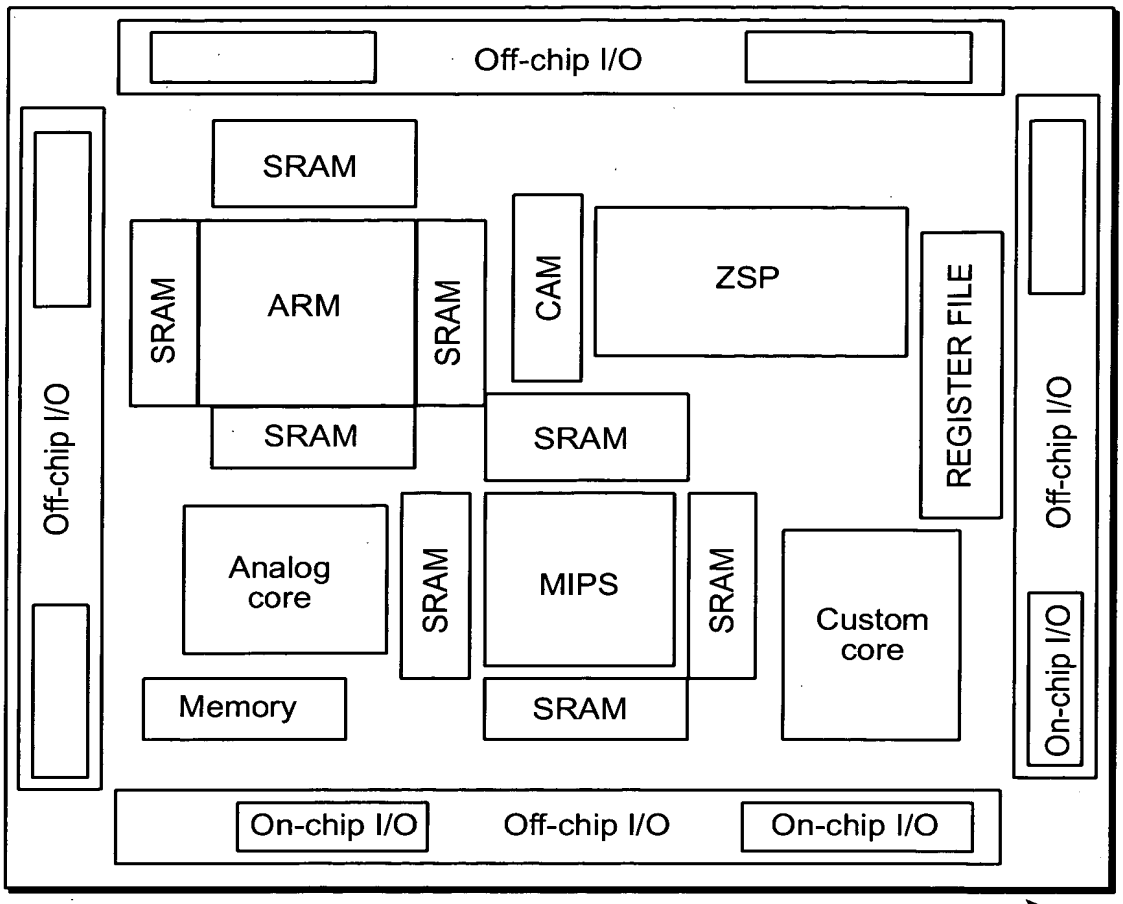
Off-chip I/O
SRAM
SRAM
ARM
SRAM
CAM
ZSP
REGISTER FILE
SRAM
SRAM
Off-chip I/O
Off-chip I/O
Analog core
SRAM
MIPS
SRAM
Custom core
On-chip I/O
Memory
SRAM
On-chip I/O
Off-chip I/O
On-chip I/O
200

FIG._2

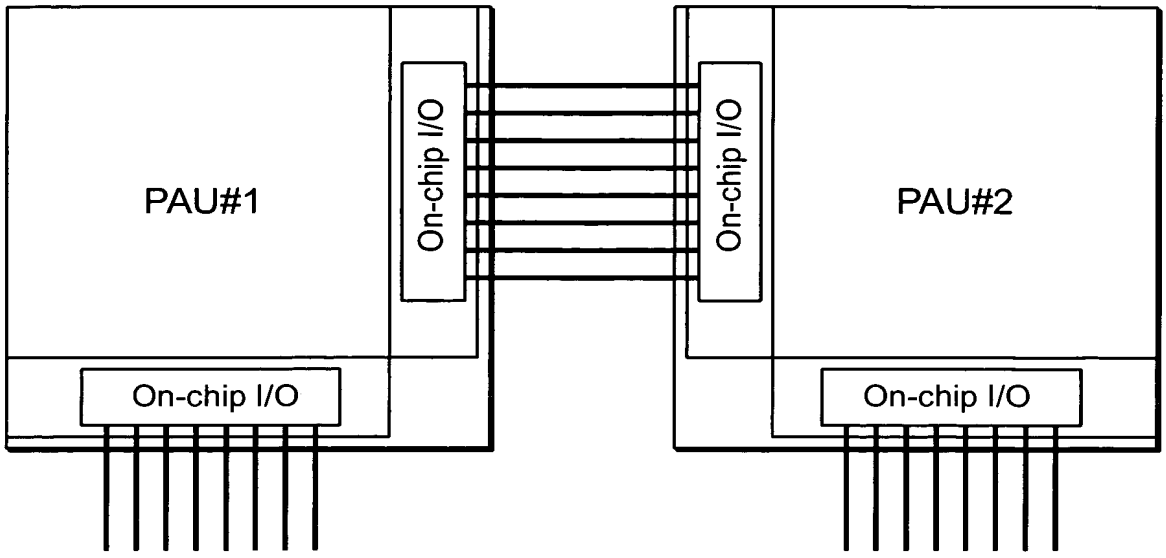
PAU#1
On-chip I/O
On-chip I/O
PAU#2
On-chip I/O
On-chip I/O

FIG._3

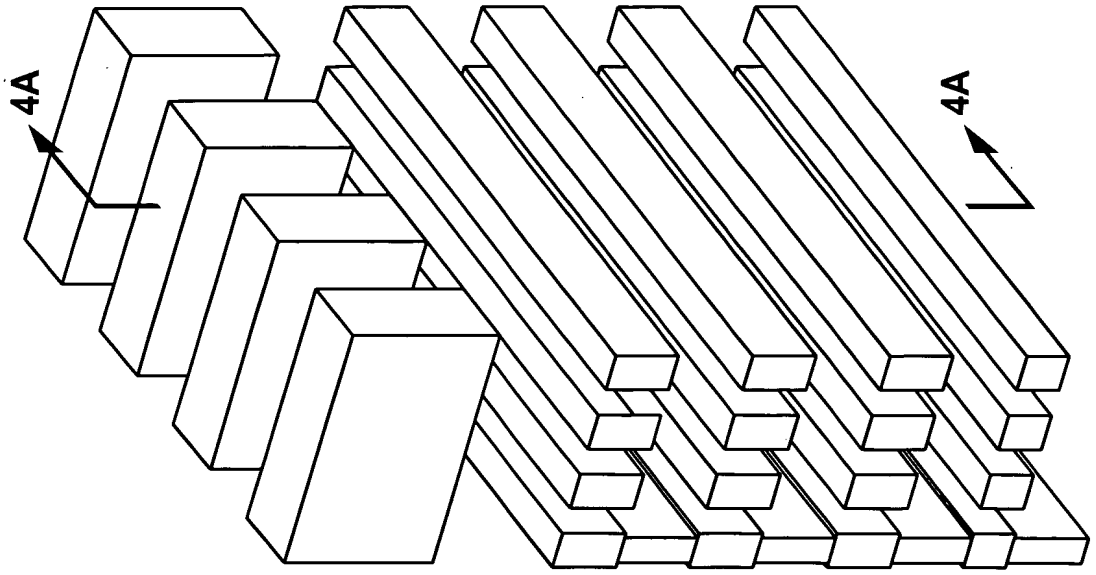

FIG._4C

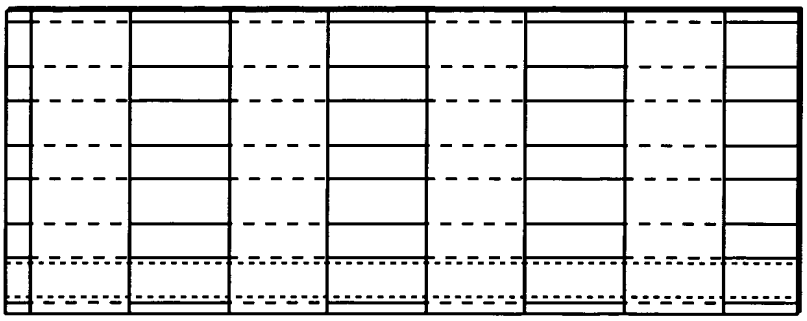

FIG._4B

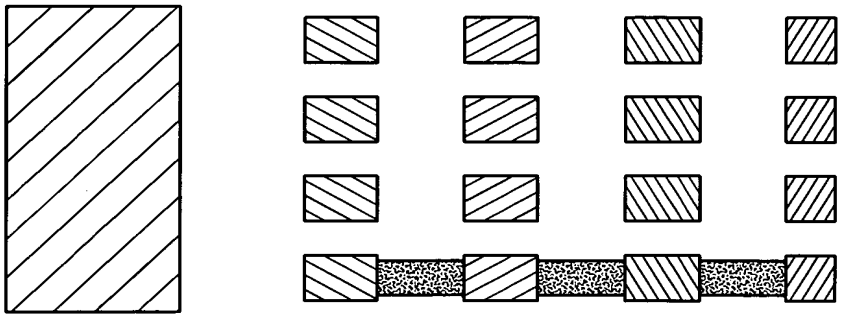

FIG._4A

Interconnect Layer Comparison

Layer	Advantages (+)	Disadvantages (-)
Bumping metal Cu	R very low; Units testable; Die seal not compromised; Unlimited array size;	Tied to flip chip; Lines wide;
Pad Metal Al	R low; Non low K; Laser programmable;	Array size limit; Smear; No unit test;
Within IC Cu	Fine line; Multi-layer	Die seal integrity; Array size limit; No unit test;
Poly	Fine line; Robust; No smear;	High R; Array size limit; No unit test;
Silicon	Medium Line; Robust; Minimal qualification needed;	Very high R; Repair difficult; Array size limit; No unit test;

FIG._5

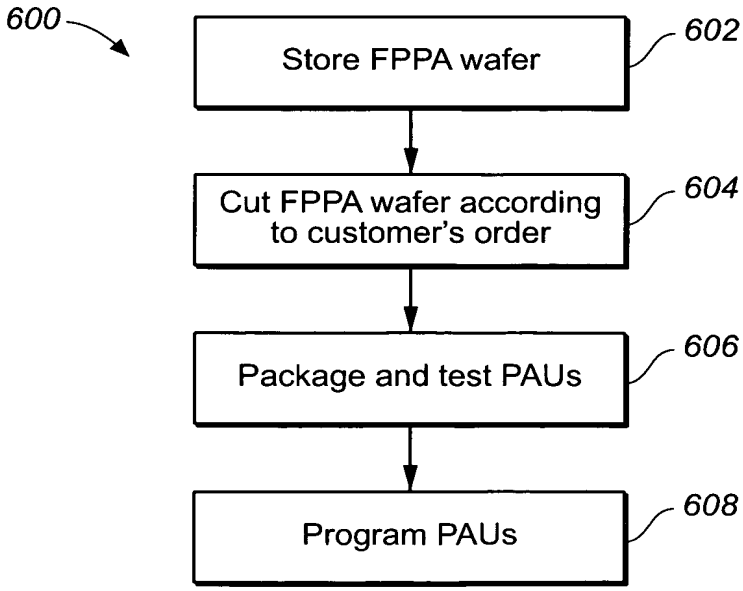

FIG._6